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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,814	02/27/2002	Joseph Francis Mann	01AB162	6548

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,814	MANN ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated October 16, 2006.

2. Claims 1-24 are presented for examination.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "to select between different external memory set-up data needed to communicate with different types of external memory"; "a non-volatile memory holding a program that when executed determines a type of memory connected to the external memory interface and from that determination selects from different methods to communicate with that external memory" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1, 12 and 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant did not disclose the subject matter of "select[ing] between different external memory set-up data needed to communicate with different types of external memory" and " a program that when executed determines a type of memory connected to the external memory interface and from that determination selects from different methods to communicate with that external memory". Regarding claims 1 and 12, the original specification discloses that the claimed invention is able to work with different types external memory by accessing setup data that describe the external memory to be accessed in terms of dynamic/static, speed, size, etc. [paragraph 0021-22 of pg. 5] It is not clear how the claimed invention would be able to select the appropriate set-up data without knowing the type of external memory [i.e., it is the set-up data that dictates the type of external memory; e.g., if the external memory type is dynamic, it is not known how the set-up data of static can be selected]. Regarding claim 24,

Examiner was not able to find the different methods of communication that are available once the external memory type has been determined. Examiner will take the position that the set-up data determines the external memory type in order to apply prior art.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3-6, 10-12, 14-16, 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Fullam et al., US Patent 5802550, hereinafter Fullam.

8. In re claim 1, Fullam discloses an integrated processor system [fig.3] comprising:

- A common integrated circuit substrate [col.6, ll.60-63] holding each of:
  - A processing unit for performing arithmetic and logical operations [52].
  - At least one internal system storage structure selected from the group consisting of caches, buffers, and registers [54].
  - An external memory interface [col.6, ll.55-57] for connecting to an external memory [58] not on the common substrate.
- Wherein the processing unit [52] executes at least a portion of a bootstrap program [boot process] to select between different external memory setup data [e.g., speed configuration data associated with different external memory] needed to communicate with different types of external memory while using the at least one internal system storage structure for temporary storage without access to external memory [col.7, l.27 – col.8, l.6; e.g., high

speed data with particular cycles related to wait time would not work with "slow" external memory].

9. As to claims 3 and 14, Fullam discloses a memory interface [56] for communicating with external memory [58] and wherein the processing unit [52] executes at least a portion of the bootstrap program [boot process] to provide for the acquisition of external memory setup data [default from 54] required for the memory interface to initiate communication with external memory [col.7, ll.39-50].

10. As to claims 4 and 15, Fullam discloses, a network interface and wherein the processing unit executes at least a portion of the bootstrap program to provide for the acquisition of the external memory setup data through a network connection [col.7, ll.39-50; configuration data stored in external 64 accessed through network].

11. As to claims 5 and 16, Fullam discloses, wherein the external memory includes non-volatile memory [64] and volatile memory [58] and wherein the processing unit executes at least a portion of the bootstrap program to provide for the acquisition of the external memory setup data for the external volatile memory from the external non-volatile memory [col.3, ll.59-63; col.7, ll.39-50].

12. As to claim 6, Fullam discloses, comprising wherein the external non-volatile memory is flash memory [col.7, ll.41-42].

13. As to claims 10 and 20, Fullam discloses, wherein the processing unit further executes at least a portion of the bootstrap program to store the memory setup data in the memory interface [54 part of 56] and then to execute a program contained in external memory [col.1, ll.25-50; col.7, l.38 – col.8, l.19].

14. As to claims 11 and 21, Fullam discloses, wherein the memory setup data is selected from the group consisting of: memory type as static or dynamic, memory speed, memory size, memory parity, and memory timing [col.3, ll.47-58; col.7, ll.11-26; col.9, ll.5-7].

15. In re claim 12, Fullam discloses each and every limitation of the claim, as discussed above in reference to claim 1. Fullam discloses the integrated processor system; therefore, Fullam discloses the method of operating the integrated processor system.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 2, 7, 13, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fullam as applied to claims 1 and 3 above, and further in view of Kao et al., US Patent 4720812, hereinafter Kao.

18. Fullam taught each and every limitation as discussed above. Fullam did not disclose explicitly communicating electrical signals with non-memory external devices.

19. In re claims 2 and 13, Kao disclose an integrated processor system [fig.3] comprising interface circuits [inherently some interface circuit in the broadest interpretation is needed for communication] for communicating electrical signals [i/o control signals] with non-memory external devices [peripheral devices] [col.6, ll.19-40].

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Fullam and Kao before him at the time the invention was made, to modify the integrated

processor system taught by Fullam to include the well known teachings of Kao, as the use of non-memory external devices is very well known and suitable for use with the integrated circuit of Fullam. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well known way to expand an integrated circuit's peripheral functions.

21. In re claims 7 and 17, Fullam discloses, wherein the processing unit includes an address translation table mapping processing unit addresses to addresses of the external memory [col.6, l.39 – col.7, l.10] and Kao discloses, wherein the processing unit executes at least a portion of the bootstrap program to make a temporary address translation table in a buffer memory [col.7, ll.37-42] so as to make the cache memory [56] available for temporary storage [col.9, ll.5-42].

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Fullam and Kao before him at the time the invention was made, to modify the integrated processor system taught by Fullam to include the teachings of Kao, in order to obtain the claimed integrated circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase the address space accessible by the processor [Kao: col.3, ll.49-63].

23. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fullam as applied to claim 1 above, and further in view of Devereux, US Patent 6671779.

24. In re claims 8 and 18, Fullam taught each and every limitation as discussed above. Fullam discloses the integrated processor system wherein the system storage structure is a cache memory [54] and wherein the processing unit executes at least a portion of the bootstrap program

to read arbitrary data into the cache memory [col.7, ll.39-50]. Fullam did not disclose locking the cache memory against further reading or writing to external memory.

25. Devereux discloses an integrated processor system [fig.3] wherein the system storage structure is a cache memory [30'] and wherein the processing unit [10] executes at least a portion of the bootstrap program to read arbitrary data [data values for interrupts] into the cache memory and then to lock the cache memory against further reading or writing to external memory [80] so that it may be used as variable storage for further execution of the bootstrap program [col.7, ll.36-49].

26. It would have been obvious to one of ordinary skill in the art, having the teachings of Fullam and Devereux before him at the time the invention was made, to modify the integrated processor system taught by Fullam to include the teachings of Devereux, in order to obtain the claimed integrated processor system. One of ordinary skill in the art would have been motivated to make such a combination as it provides speed benefits without data corruption [Devereux: col.7, ll.36-49].

27. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fullam as applied to claim 3 above, and further in view of Little et al., US Patent 6272637, hereinafter Little.

28. In re claims 9 and 19, Fullam taught each and every limitation of the claim, as discussed above in reference to claim 3. Fullam discloses wherein the processing unit executes at least a portion of the bootstrap program to store the memory setup data in the memory interface [54 part of 56] [col.1, ll.25-50; col.7, l.38 – col.8, l.19]. Fullam did not disclose explicitly loading additional programs for execution into external memory.

29. Little discloses an integrated processor system [fig.3] wherein the processing unit loads additional programs for execution into external memory [130] [col.5, ll.39-51].

30. It would have been obvious to one of ordinary skill in the art, having the teachings of Fullam and Little before him at the time the invention was made, to modify the integrated processor system taught by Fullam to include the teachings of Little, in order to obtain the claimed integrated processor system. One of ordinary skill in the art would have been motivated to make such a combination as it provides secured processing of information [Little: col.1, ll.39-59].

31. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fullam as applied to claim 1 above, and further in view of Gupta, US Patent 6577158.

32. Fullam taught each and every limitation as discussed above. Fullam discloses a program [boot process] that when executed determines a type of memory connected to the external memory interface and from that determination selects from different methods to communicate with that external memory [e.g., speed configuration data associated with different external memory and how fast to communicate], the program executing using the internal system storage structure for temporary storage without access to external memory for temporary storage [col.7, l.27 – col.8, l.6; e.g., high speed setup data with particular cycles related to wait time determines particular external memory]. Fullam did not disclose explicitly the bootstrap program is stored in a bootstrap memory also on the common integrated circuit substrate.

33. In re claims 22 and 23, Gupta discloses an integrated processor system [fig.1] wherein the bootstrap [startup] program is stored in a bootstrap memory [140] also on the common integrated circuit substrate [105] [col.5, ll.20-31].

34. In re claim 24, Gupta discloses an integrated processor system [fig.1] comprising a common integrated circuit substrate [105] holding a non-volatile memory [140] holding a program [startup analogous to Fullam boot process] [col.5, ll.20-31].

35. It would have been obvious to one of ordinary skill in the art, having the teachings of Fullam and Gupta before him at the time the invention was made, to modify the integrated processor system taught by Fullam to include the teachings of Gupta, in order to obtain the claimed integrated processor system. One of ordinary skill in the art would have been motivated to make such a combination as it reduces the size and power consumption as well as manufacturing costs [Gupta: col.1, ll.27-38].

Response to Arguments

36. Applicant's arguments filed October 16, 2006 have been fully considered but they are not persuasive.

37. Applicant argues that "Fullam does not select between different types of memory but always assumes a universal memory standard". Firstly, Fullam is supposed to work with different types of memory [i.e., not ***select*** the type of memory that the circuit can work with, which would defeat the objective of being flexible]. Secondly, Fullam reads the configuration data from 64 to determine the particular speed/type of memory, which does not indicate that it assumes a universal memory standard [col.7, l.27 – col.8, l.6].

38. Applicant argues that "there is no indication in Fullam that the bootstrap memory of Fullam uses the parameter memory 54 for 'temporary storage'". Examiner disagrees and submits that Fullam clearly discloses that 54 is adjusted according to the setup data obtained from 64

[col.7, ll.27-50]. Absent any explicit definition regarding "temporary", Examiner submits that the adjustable 54 constitutes a "temporary" storage.

39. Applicant argues that "Fullam limits the embedded processor to only communicating with memory types that have a common default mode... teaches away from the present invention by requiring communication with the external memory before identification of the external memory type is determined". Examiner disagrees and submits that Fullam discloses communicating with different external memory types via the configuration data stored in 64 [col.3, ll.19-31]; and booting ***may*** be done with information in the external memory with the default mode, but it is not required as Applicant alleges [col.7, ll.27-50; col.8, ll.7-19].

40. As such, Applicant's arguments are deemed not persuasive and the rejections are respectfully maintained.

Conclusion

41. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
November 3, 2006